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Control of a Three-Phase to Single-Phase Back-to-Back Converter for Electrical Resistance Seam Welding Systems

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Abstract: DC link back-to-back converters are widely used in industrial applications. This interest comes from their power factor unity capability on the utility grid and to maintain regulated output parameters, thanks to the decoupling between the grid and the load side. In this paper, a 150 KVA prototype of DC link back-to-back converter for electrical resistance seam welding applications is described. The focus of the paper is on the control strategy developed to absorb constant power from the three-phase utility grid. The key idea is to allow the voltage on the DC bus to vary in order to avoid the propagation at the input side of the pulsed power required by the load. An estimation procedure of the load parameters is presented too. The effectiveness of this control scheme has been proved by simulations and tests.

Keywords: DC-link back-to-back converters; power factor correction; three phase pulse width modulated (PWM) rectifier; parameter estimation; resistance seam welding

1. Introduction

Electrical resistance welding (ERW) systems are widely used in the metallurgical and automotive industry [1–4]. This interest for ERW systems comes from their capability to make high-speed welding with good heat concentration, without additional materials, solvents, and shielding gas. This leads to weld with high productivity, low cost, and less pollution. The basic principle of an ERW system is to weld two materials using the heat generated by the passage of an electric current through the resistance formed by the contact between two metal surfaces [2]. Resistance seam welding (RSEW) is a particular ERW process where copper electrodes are disc-shaped to allow continuous welding of materials, commonly round or rectangular steel tubing. The electrodes rotate as the material passes between them. This allows the electrodes to stay in constant contact with the material to make continuous welds. RSEW typically applies low voltages and high welding currents in the range of 100 A–100 kA [2]. The welding current is one of the most important parameters of the welding process, as the amount of heat produced is proportional to its square.

In RSEW systems, single-phase high AC welding current is preferred compared to DC current used in resistance spot welding systems due to better electrode life performance, longer welding process, and the simplicity of use of the converter [3]. To perform at the above current requirement for RSEW

power supply, a suitable high power converter is needed to feed a step-up current load transformer. The typical power converter topologies make use of an indirect voltage source configuration, made of a three-phase front-end diode rectifier with a DC-link capacitor, or thyristors with an inductor and capacitor (LC) power decoupling filter, and a pulse width modulated (PWM) single-phase inverter in both cases. However, both diode and thyristor topologies have the drawback to absorb a highly distorted current from the utility grid, and, in the case of thyristors, to draw reactive power and to create commutation line notching problems. Improvements in electromagnetic compatibility (EMC) standards proposes to solve those problems [5]. Additional PFC (power factor correction) circuits can be added to solve this problem. However, the solution proposed in this paper is to make use of a front-end PWM voltage source rectifier. Although many studies in the literature have dealt with indirect AC–AC converters with PWM rectifiers, they mainly treat the case of three-phase to three-phase conversion where constant power is transferred between the input and output side or single-phase to single-phase conversion [6–11]. Given the current and the PFC requirements for RSEW welding systems, a three-phase boost rectifier has to be used back-to-back with a single-phase voltage source inverter. This results in a three-phase to single-phase back-to-back converter topology studied in this paper. The main drawback to be taken into account for this application is that load parameters can vary in a non-linear way during the welding process [12]. This paper aims to propose a control strategy acting on the DC link voltage to absorb constant power from a three-phase grid and to deliver regulated output current and frequency to the load even in case of large load variations.

The paper is organized as follows: Section 2 presents the system topology and its mathematical description. Section 3 shows the proposed control strategy and simulations results. Section 4 shows the experimental results, and conclusions are given in Section 5.

2. System Description and Analysis

2.1. System Description

The converter schematic is shown in Figure 1. On the grid side there is a three-phase voltage source rectifier fed through coupling inductances. On the load side there is a single-phase, full bridge voltage source inverter. Both converters are controlled by PWM techniques. The DC link has been designed to allow a DC voltage variation between 650 V and 850 V, with a nominal value U_{Cnom} of 780 V. This choice allows for a variation range of the DC link large enough to guarantee the proper functioning of the boost voltage source rectifier [11]. For studying the system, the load has been modeled by an equivalent resistance and inductor (RL) circuit. This model is suitable to represent the short-circuited transformer used for the preliminary tests presented in Sections 2 and 3. The behavior of the system with the real load will be presented in the Section 4.

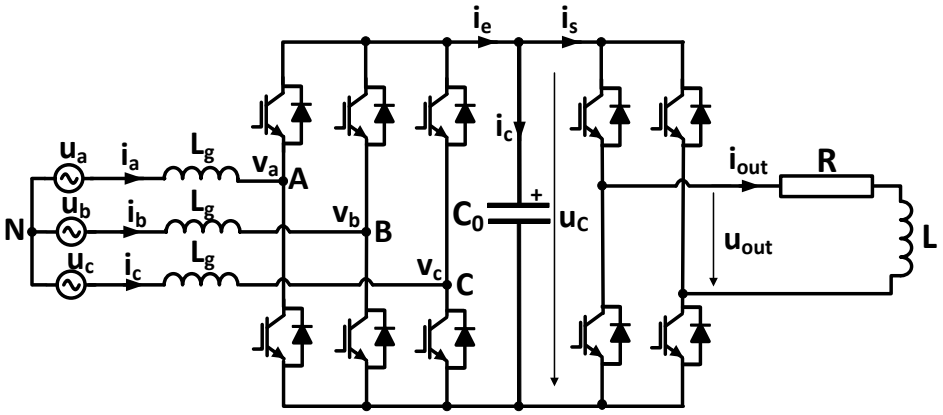


Figure 1. Three-phase to single-phase converter schematic, with the resistance and inductor (RL) equivalent load.

2.2. Mathematical Description of the System

Since the goals in this paper are to control the power factor, to regulate the DC link capacitor voltage, as well as the output current, the equations derived in this section highlight the grid currents and the capacitor voltage.

2.2.1. Pulse Width Modulated Rectifier

Let us consider a three-phase utility grid. Using Figure 1, the three-phase variables can be expressed in the synchronous rotating coordinates as:

$$\begin{aligned} u_d &= L_g \tfrac{di_d}{dt} - \omega_g L_g i_q + v_d \\ u_q &= L_g \tfrac{di_q}{dt} + \omega_g L_g i_d + v_q. \end{aligned} \tag{1}$$

The real and reactive powers supplied from the source are given by:

$$\begin{aligned} p &= \tfrac{3}{2}\left(u_d i_d + u_q i_q\right) \\ q &= \tfrac{3}{2}\left(u_d i_q - u_q i_d\right). \end{aligned} \tag{2}$$

If the d-axis of the rotating reference frame is well aligned with the AC voltage vector so that u_q = 0, the instantaneous real and reactive powers absorbed from the utility grid are given by:

$$\begin{aligned} p &= \tfrac{3}{2} u_d i_d \\ q &= \tfrac{3}{2} u_d i_q. \end{aligned} \tag{3}$$

If only real power is transferred from the grid to the DC link (i_q = 0), the power balance relationship between the AC input and DC output is given as:

$$\frac{3}{2}\hat{U}_g i_d = u_C i_e. \tag{4}$$

2.2.2. Power Pulsation Compensation

In order to perform an effective power pulsation compensation, a power decoupling capacitor voltage command has to be established to compensate for power pulsation on the load side. Let us consider the system in a sinusoidal steady-state. The current and voltage on the output side can be expressed as:

$$\begin{aligned} i_{out}(t) &= I_{out}\sqrt{2}\sin(\omega_{out} t) \\ u_{out}(t) &= U_{out}\sqrt{2}\sin(\omega_{out} t + \varphi_{out}), \end{aligned} \tag{5}$$

where U_{out} and I_{out} are the effective values of the output voltage and current, ω_{out} is the output angular frequency, and φ_{out} is the phase displacement between the two. The instantaneous power p_{out} (t) on the load is given by:

$$\begin{aligned} p_{out}(t) &= u_{out}(t) \cdot i_{out}(t) \\ &= U_{out} I_{out}\cos(\varphi_{out})[1 - \cos(2\omega_{out} t)] + U_{out} I_{out}\sin(\varphi_{out})\sin(2\omega_{out} t), \end{aligned} \tag{6}$$

and the instantaneous active power p_{active_inst} (t) on the load is:

$$p_{active\_inst}(t) = U_{out} I_{out}\cos(\varphi_{out}) \cdot [1 - \cos(2\omega_{out} t)]. \tag{7}$$

The instantaneous active power varies at two times the output current frequency. If the PFC rectifier is forced to absorb a constant power from the utility, the voltage variation on the DC link will follow the frequency of the instantaneous active power. As a matter of fact, assuming that the constant

power supplied by the utility is equal to the active power P_{active} of the load, neglecting the losses on the rectifier and inverter, we have:

$$\begin{aligned} P_{grid} &= P_{active} \\ &= U_{out} I_{out} \cos(\varphi_{out}). \end{aligned} \tag{8}$$

From the power balance between the input and output, the power on the DC link capacitors can be expressed as:

$$\begin{aligned} p_{cap}(t) &= P_{active} - p_{out}(t) \\ &= U_{out} I_{out} \cos(2\omega_{out} t + \varphi_{out}) \\ &= u_C(t) \cdot C_0 \frac{du_C(t)}{dt}. \end{aligned} \tag{9}$$

The voltage of the capacitor tank can be obtained by integrating Equation (9):

$$u_C^2(t) = \frac{U_{out} I_{out} \sin(2\omega_{out} t + \varphi_{out})}{C_0 \omega_{out}} + cst \tag{10}$$

where *cst* is an integration constant. Supposing that when $t = 0$, the voltage across the capacitor tank has its nominal value U_{Cnom}, we can rewrite Equation (10) as:

$$u_c(t) = \sqrt{U_{Cnom}^2 + \frac{U_{out} I_{out}}{C_0 \omega_{out}} \sin(2\omega_{out} t + \varphi_{out}) - \frac{U_{out} I_{out}}{C_0 \omega_{out}} \sin(\varphi_{out})} \tag{11}$$

Equation (11) highlights the variation of the DC link voltage due to the single-phase load. Some studies have addressed this DC link voltage ripple issue by adding a buffer circuit into the DC link to decouple the power ripples [13], or by using a ripple port module for ripple cancellation purposes [14]. However, using such solutions in our case will increase the number of components, the complexity, and the cost of the system. Moreover, given that, in our application, the output current frequency is allowed to vary within a range depending of the material to weld, many buffer circuits corresponding to each possible frequency of the output current would be necessary. In [15], it has been proposed to mitigate the propagation of the power fluctuation of a variable speed wind turbines on the utility side by allowing the DC link voltage to vary within a certain range. Such an approach will be used in this paper to compensate the power pulsation due to the single phase load. For that, Equation (11) provides a suitable DC link reference voltage to use.

3. Control Strategy

3.1. Unity Power Factor Formulation

Power quality is performed when the total harmonic distortion (THD) generated by the converter at the point of common coupling is less than 5% with a power factor (PF) greater than 0.99 [16]. The power factor calculation can be performed using Equation (12), where φ represents the phase displacement between the fundamental of the current and voltage:

$$\mathrm{PF} = \frac{\cos(\varphi)}{\sqrt{1 + \mathrm{THD}^2}} \tag{12}$$

If the load parameters of the converter are constant and well-known, the PF requirement can be simply achieved by providing the appropriate current reference to the PFC rectifier. The most commonly used control strategy for PFC rectifier is the voltage-oriented control (VOC) [11]. It is based on an external DC voltage control loop and an internal current decoupled control loop. The inner closed-loop current control is done in a rotating reference frame. The three-phase measured values are converted to an equivalent two-phase stationary system $\alpha\beta$ and are then transformed to the rotating coordinate system dq using Clark and Park transformations. Proportional and integral (PI) regulators

are used on DC values i_d and i_q presented in Equation (1), to eliminate steady-state error. A unity power factor is obtained by forcing the current reference value i_{qref} to be zero, while i_{dref} is set to control the active power flow. The output signals from the PI controllers after dq to $\alpha\beta$ transformation are used for switching signal generation by a space vector modulator (SVM). A SVM is chosen to generate the PMW rectifier command because it allows to extend the linear domain of about 15%. In the case of the converter studied here, unit power factor can be achieved by using the same approach and by setting the DC link voltage reference to follow Equation (11).

3.2. Control of the Output Current

The control of the output current is performed using a classical current loop. This output control loop is decoupled from the rectifier control loop due to the capacitor tank. The current flowing through the load inductor is measured and compared to its reference value. A PI controller uses the error signal to provide the voltage command which will be compared to the inverter carrier signal in order to generate the PWM commands for the inverter switches.

3.3. Proposed Estimation of Equivalent Load Parameter's Values

When load parameters vary, the reference current i_d varies around its average value and the amplitude of the ripple is related to the gap between the preset values of the load parameters and their real values. The ripple of the reference current i_d around its average value leads to a variable power absorption on the utility grid and increases the harmonic distortions of the grid current. Then, the control strategy has to be adapted to cope with those variations.

The relationship between the voltage across the capacitors and the phase displacement on the output side is known from Equation (11). Given that the phase displacement is directly related to the resistance and inductance of the load, it is possible to handle their variations by providing the appropriate DC bus voltage reference to the PFC rectifier. This requires a suitable estimation of the equivalent load parameters.

As previously mentioned, the load is modelled by the series connection of a resistance and an inductance. The value of these two parameters must be estimated. In order to evaluate the value of the resistance, the active power absorbed by the load can be used. The single-phase inverter output current and voltage are measured. Active power P_{active} is evaluated each period and the actual value of resistance can be obtained using Equation (13):

$$R = \frac{P_{active}}{I_{out}^2} \tag{13}$$

If the actual value of the resistance is known, the actual value of the inductance can be estimated using Ohm's law, as in Equation (14):

$$L = \frac{\sqrt{\frac{U_{out}^2}{I_{out}^2} - R^2}}{\omega_{out}} \tag{14}$$

The equivalent R, L estimation algorithm is shown in Figure 2. To optimize the digital signal processor (DSP) computational load, the proposed strategy will update the estimated parameters once each period. Given that the measures might be prone to noise, measurements are first filtered to reject any disturbances before being used in the estimation scheme.

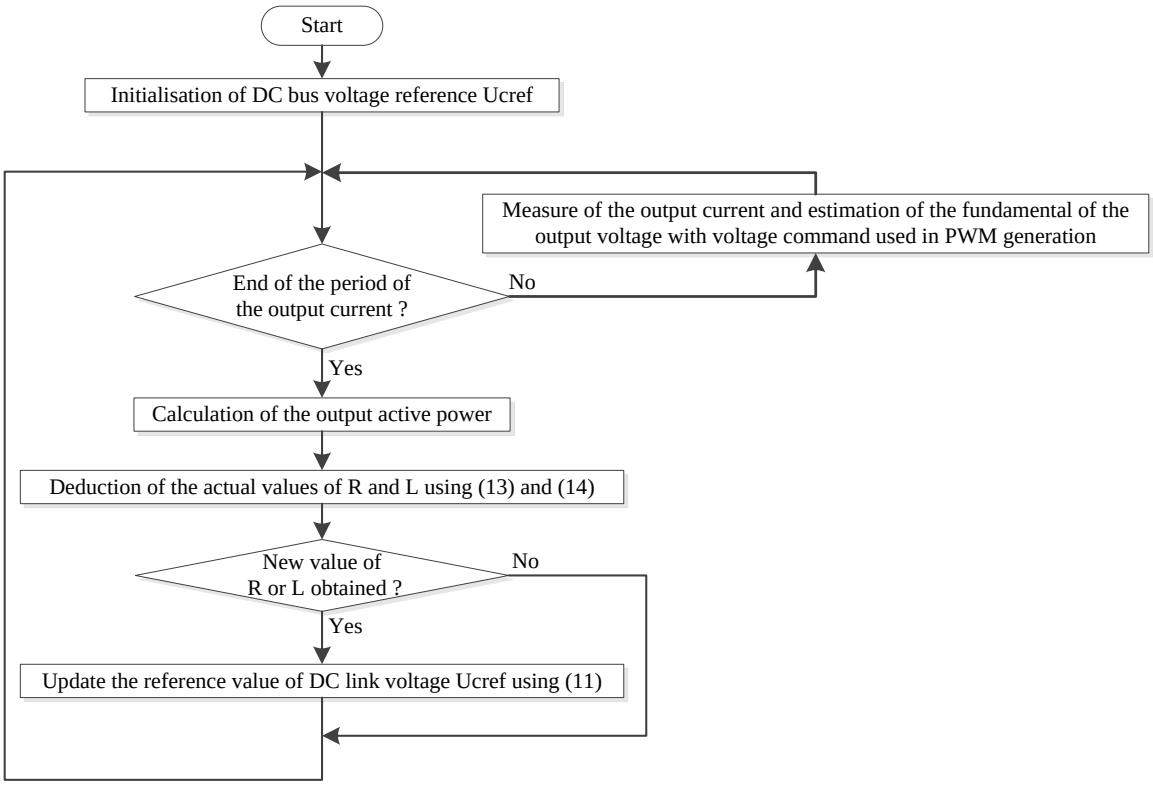


Figure 2. Flowchart of the *R, L* estimation algorithm.

3.4. Tuning of the Controllers

In order to eliminate the steady—state error, PI controllers are used at all control stages. The PI controller transfer function is given in the Equation (15) where T_n and T_i are the time constants of the integral correlation and the integral action, respectively:

$$C(s) = \frac{1 + sT_n}{sT_i} \tag{15}$$

Using Equation (1), and taking into account the PWM modulator model, the current control loop can be equivalently represented by Figure 3b, where T_{PE} represents the switching period and the sum of all of the parasitic process time constants. The DC link voltage is regulated using the active power carrying component of the grid current. Given Equation (4), the current flowing through the DC link capacitor can be expressed as:

$$i_c = C_0 \frac{du_C(t)}{dt} = \frac{3\hat{U}_g i_d}{2u_C} - i_s \tag{16}$$

Using Equation (16), the DC link voltage control loop can be equivalently represented by Figure 3a. By using the same approach, the output current control loop can be represented by Figure 3c. Once the control loops are obtained, the coefficients of the controller can be designed using modulus and symmetrical optimum, such as that presented in [17]. Table 1 summarizes the obtained controller parameters.

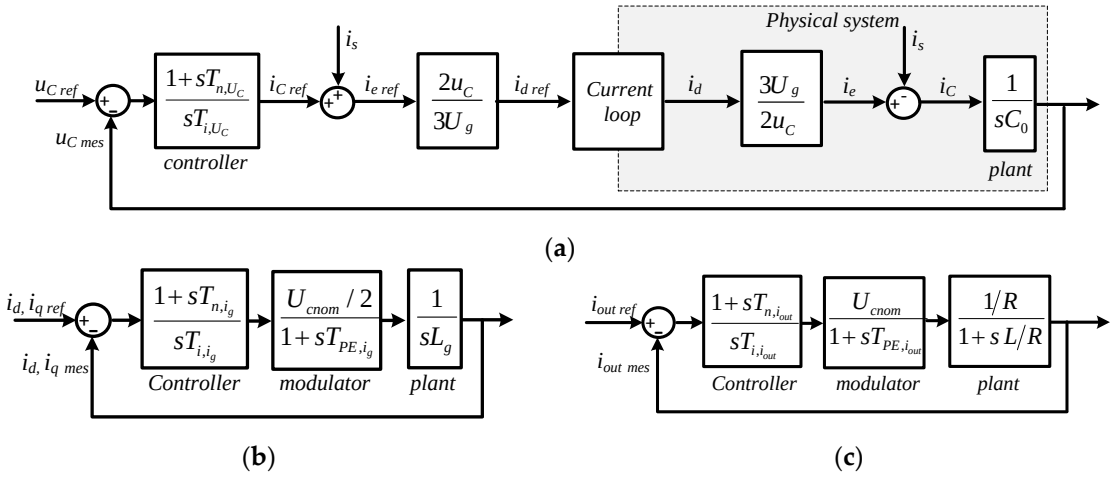


Figure 3. Equivalent representation of the control loops. (**a**) DC link voltage control loop; (**b**) the grid current control loop; and (**c**) the output current control loop.

Table 1. Proportional and integral (PI) controller's parameters.

Control Section	Open Loop Transfer Function	T_n	T_i	Criterion Used
Grid current control loop	$\frac{\left(1+sT_{n,i_g}\right)\cdot U_{cnom}}{2\cdot s^2\cdot T_{i,i_g}\cdot L_g\cdot\left(1+sT_{PE,i_g}\right)}$	$4\cdot T_{PE,i_g}$	$\frac{4\cdot T_{PE,i_g}^2\cdot U_{cnom}}{L_g}$	Symmetrical optimum
DC link voltage control loop	$\frac{1+sT_{n,u_C}}{s^2\cdot T_{i,u_C}\cdot C_0\left(1+2sT_{PE,i_g}\right)}$	$8\cdot T_{PE,i_g}$	$\frac{32\cdot T_{PE,i_g}^2}{C_0}$	Symmetrical optimum
Output current control loop	$\frac{\left(1+sT_{n,i_{out}}\right)\cdot U_{cnom}}{s\cdot T_{i,i_{out}}\cdot R\cdot\left(1+sT_{PE,i_{out}}\right)\left(1+s\frac{L}{R}\right)}$	$\frac{L}{R}$	$\frac{2\cdot T_{PE,i_{out}}\cdot U_{cnom}}{R}$	Modulus optimum

3.5. Overview of the Control System

The block diagram of the whole structure of the controller is presented in the Figure 4. A closed loop phase locked loop (PLL) module has been added for the synchronization to the grid, such as that in [18].

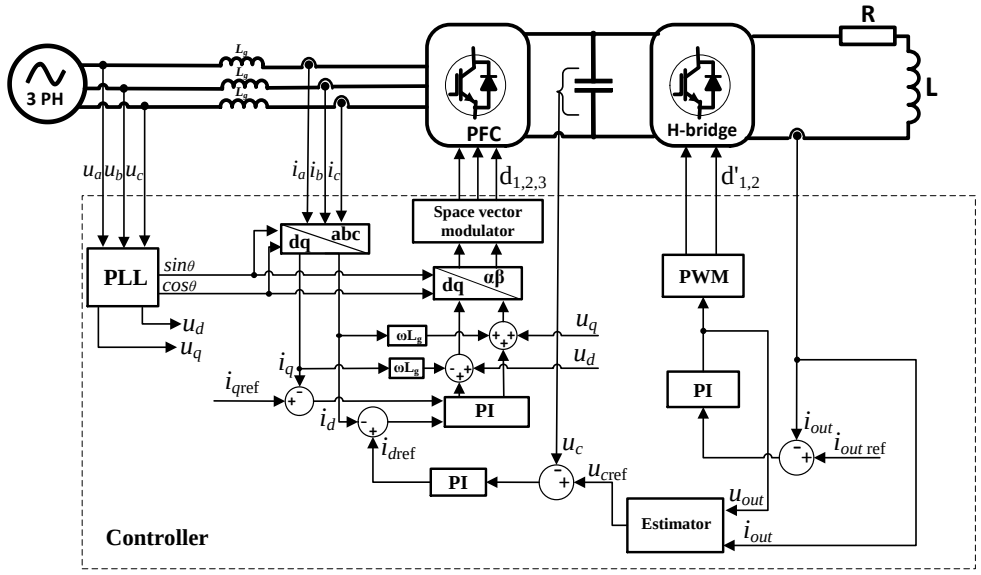


Figure 4. Structure of the controller. Proportional and integral (PI) denotes proportional and integral controller.

3.6. Simulations Results

Circuit parameters are presented in Table 2. Simulations are performed using PLECS© software [19]. The active rectifier is controlled in the rotating frame *dq* as mentioned in the previous sections. A unit power factor is then obtained by forcing the current reference value i_{qref} to be zero, while i_{dref} is set to control the active power flow.

Table 2. System parameters used in simulation and experimental setup. PFC: Power factor Correction.

Symbol	Quantity	Value
U_{grid}	Effective value of the grid voltage	230 V
C_0	DC-link Capacitor tank	19.8 mF
R	Theoretical load resistance	56 mΩ
L	Theoretical load inductance	512 µH
f_{s_PFC}	Switching frequency of the PFC rectifier	10 kHz
f_{s_INV}	Switching frequency of the inverter	5 kHz
f_{ech}	Sampling frequency	10 kHz
f_{grid}	Grid frequency	50 Hz
I_{out}	Effective value of the output reference current	848 A
f_{out}	Output frequency	60 Hz
L_g	Grid coupling inductance	123 µH
U_{cnom}	Nominal DC bus voltage	780 V

3.6.1. Constant Load Simulations

Figure 5 presents a simulation where the load parameters are constant. In this simulation, the PFC rectifier has been set to follow the theoretical DC voltage ripples expressed in Equation (11) (Figure 5d). One can see in this figure that the pulsed power on the load side does not affect the feeder side. A constant power is supplied by the grid because the variations on the reference current i_d shown in Figure 5b are very small (less than 3% between instants t = 0.16 s and t = 0.18 s) and the grid currents present regular amplitudes (Figure 5a). Output current is well regulated (Figure 5c) and the power factor calculated using Equation (12) is about 0.99 with a THD = 1.77% (Figure 5e).

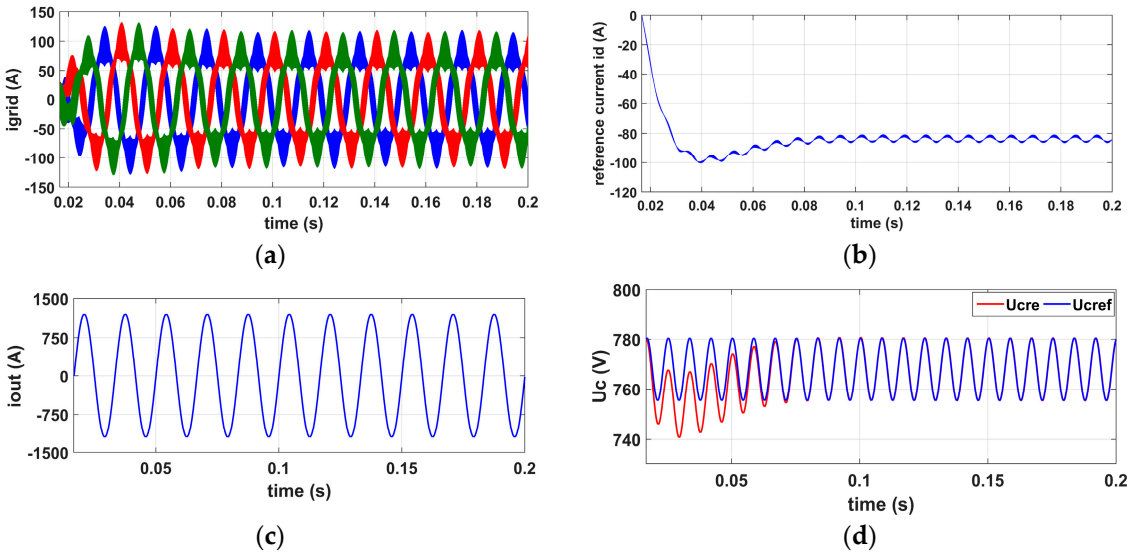
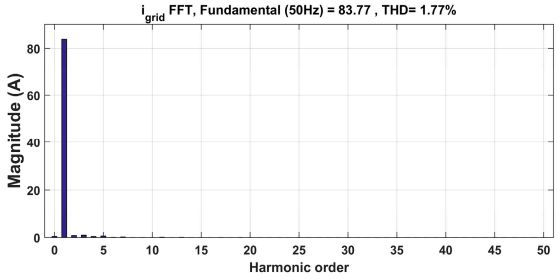


Figure 5. *Cont.*

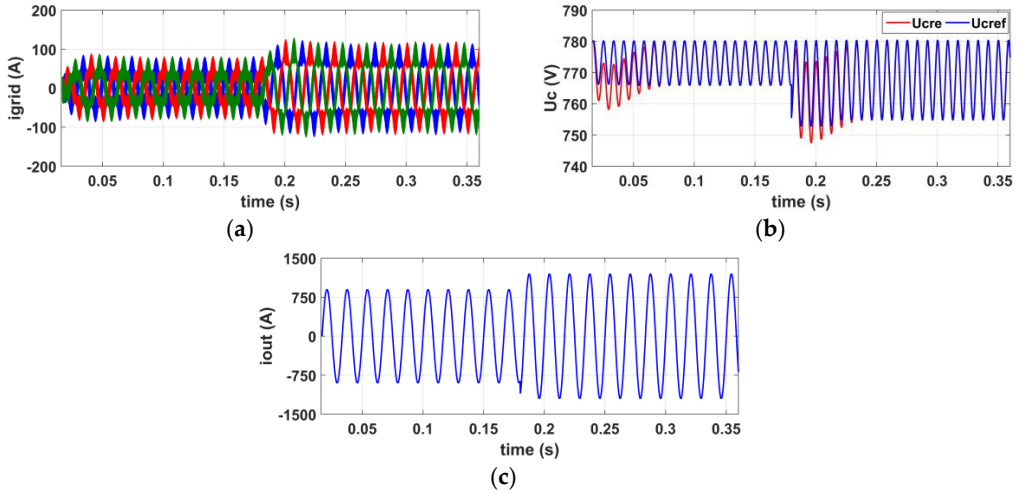


(**e**)

Figure 5. Waveforms on the converter with constant load where output power S_{out} = 140 KVA. (**a**) Grid currents; (**b**) reference current i_d in the dq frame; (**c**) output current i_{out}; (**d**) DC bus voltage. U_{Cre} = real value (red trace), U_{Cref} = reference value (blue trace); and (**e**) the harmonic spectrum of one of the grid currents.

3.6.2. Step Change in the Output Current Reference

A second simulation shows the response of the controller with an output current reference step. Simulations results are presented in the Figure 6. At t = 0.18 s, the output current reference amplitude steps from 900 A to 1200 A. Good controller dynamics can be observed.



(**a**) (**b**) (**c**)

Figure 6. Waveforms on the circuit with change in the reference of the output current. (**a**) Grid currents; (**b**) DC bus voltage. U_{Cref} = reference value (blue trace), U_{Cre} = real value (red trace); (**c**) The output current i_{out}.

3.6.3. Step Change of Output Parameter Values

A third simulation shows the behavior of the controller with a step change of the load resistance and inductance. The left column of the Figure 7 presents the waveforms obtained without tracking the load parameter, while the right column of the Figure 7 shows the waveforms with the proposed control scheme, including an estimation of load variations. At the beginning of both simulations, the theoretical load resistance and inductance in the controller are equal to their actual circuit values. At t = 0.10 s, the load resistance is changed from R to $2.5R$. At t = 0.183 s, the load inductance is changed from L to $2L$, and at t = 0.275 s, the load resistance is changed from $2.5R$ to $0.8R$. The actual and estimated resistance and inductance values are shown in Figure 7b,d, respectively. The estimation delay is, at most, one period of the output current. The choice to update the load parameters at the end of each period of the output current instead of making a sliding average is made to be as close as possible to the hardware implementation. In fact, the frequency of the output current can be set

in a range of 5–80 Hz depending on the type of the material to weld. Making a sliding average at low frequency might cause an overflow of the microcontroller's memory due to the sampling period. However, this update delay does not significantly affect the control scheme.

When the controller does not take into account the load variations (left column of Figure 7), grid currents present harmonic distortions and irregular amplitudes (Figure 7e,k), leading to fluctuating power supplied by the three phase grid. This results in a large ripple of the reference current i_d around its mean value (Figure 7g). For example, the i_d reference current's ripples between instants t = 0.32 s and t = 0.36 s is about 51.4%, leading to a power factor of about 0.90 with a THD = 38.91%. On the other hand, when the load parameters are estimated and are included in the calculation of the DC bus voltage reference (Figure 7j compared to Figure 7i), their variations do not affect grid currents. This leads to regular amplitudes of the latter (Figure 7f) and, hence, constant power is drawn from the grid. The i_d reference current's ripples around its mean value between instants t = 0.32 s and t = 0.36 s is now about 4.6%, corresponding to a reduction of about 91% and resulting to a power factor of about 0.99 with a THD = 6.88%. The THD has, thus, been reduced by about 82%. This confirms the effectiveness of the proposed adaptive scheme.

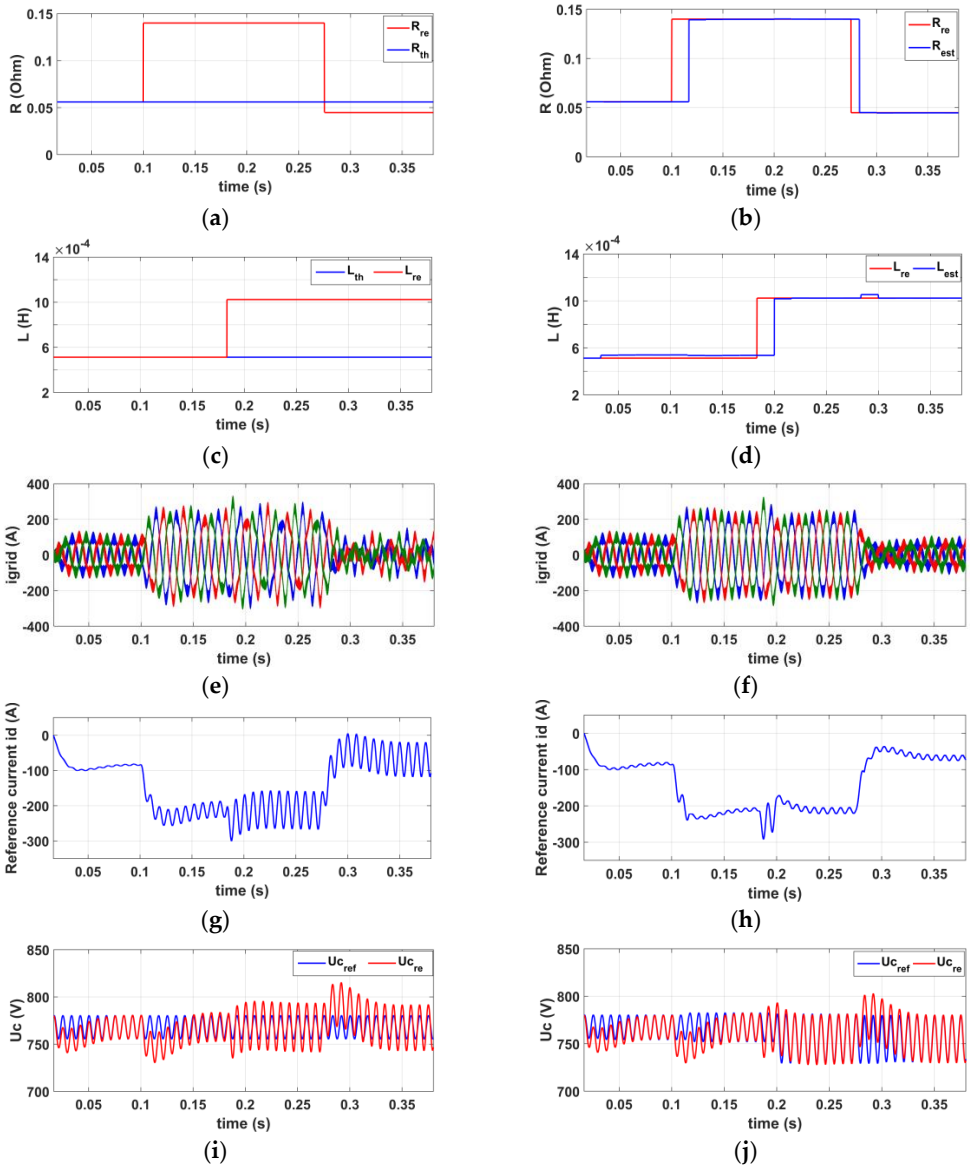


Figure 7. *Cont.*

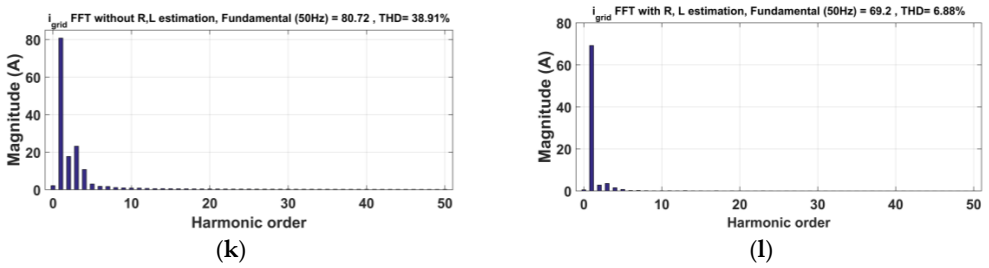


Figure 7. Simulations results of a step change of load parameters. (**a**) Real and theoretical load resistance; (**b**) real and estimated load resistance; (**c**) real and theoretical load inductance; (**d**) real and estimated load inductance; (**e**) grid currents without estimation scheme; (**f**) grid currents with estimation scheme; (**g**) reference current i_d without estimation scheme; (**h**) reference current i_d with estimation scheme; (**i**) DC bus voltage reference and real DC bus voltage without the estimation scheme; (**j**) DC bus voltage reference and real DC bus voltage with the estimation scheme; (**k**) harmonic spectrum of one of the grid currents without the estimation scheme; and (**l**) harmonic spectrum of one of the grid currents with estimation scheme.

4. Experimental Results

In order to verify the expected behavior of the control scheme, a full-scale prototype has been built. The specifications of the experimental setup are the same as in Table 2. The layout of the prototype is shown in Figure 8. This prototype consists of a capacitor tank designed for a voltage up to 900 VDC, a three-phase rectifier and a full bridge inverter both using Fuji insulated gate bipolar transistor's (IGBT) (6MBI450V-120-50) [20], a three-phase coupling inductance and a load. The control of the whole system shown in Figure 4 has been implemented on a single Texas Instruments TMS320F28335 "Delfino" microcontroller [21]. Two series of tests are presented in the following sections. The first set of tests has been done on a full scale dummy load and the second set of tests has been done on a resistance seam welding system.

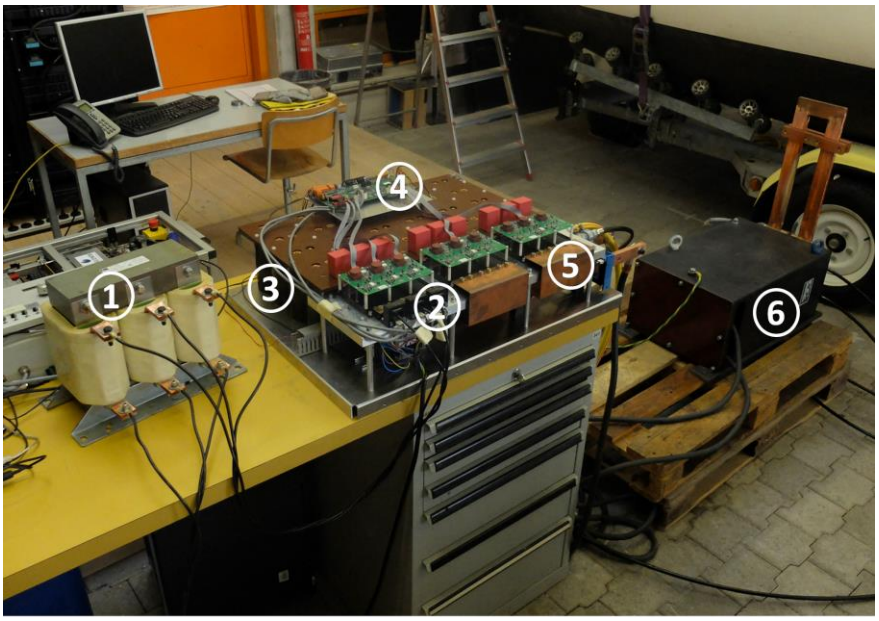


Figure 8. Prototype layout: (**1**) Three-phase coupling inductance; (**2**) Three-phase PFC rectifier; (**3**) DC-link capacitor; (**4**) Control board; (**5**) Inverter; and (**6**) load transformer.

4.1. Tests on a Dummy Load

The dummy load used consists of a short-circuited high-power transformer with a 1:30 turn ratio. Figure 9a–c show the waveforms of a test performed at I_{out} = 848 A and S_{out} = 144 kVA. Two phases of the grid current and one phase of the grid voltage are presented in Figure 9a. The voltage (pink trace) and its corresponding current (blue trace) are perfectly synchronized. In this case, the power factor calculated using Equation (12) is about 0.99. Grid currents show regular amplitudes. Figure 9b shows the DC bus voltage for the same operating point as above. The ripple ratio of DC bus voltage is a little bit higher (2%) than the simulation results shown in Figure 5d. This is due to the losses on the inverter and to component tolerances. Figure 9c presents the harmonic spectrum of the grid current presented in Figure 9a (blue trace). One can denote a low harmonic content with a THD of about 9.69%. Figure 9d shows the output current at I_{out} = 106 A, S_{out} = 2.25 kVA.

Figure 10 presents waveforms plotted with samples recorded using the microcontroller to test the response of the controller with an output current reference step and the load parameter's estimation scheme. At t = 0.05 s, the amplitude of the output current reference steps from 450 A to 1200 A (exactly at the beginning of the output current period), and at t = 0.12 s the amplitude is changed from 1200 A to 450 A (generic instant within a period). Figure 10a,b present the load resistance and inductance estimations over time. A smooth transition occurs after the first step. A peak is observed on the output voltage (Figure 10d) after the second step. However, the controller effectively handles the instantaneous variations of the output current reference. Test results demonstrate the correct behavior of the proposed control strategy.

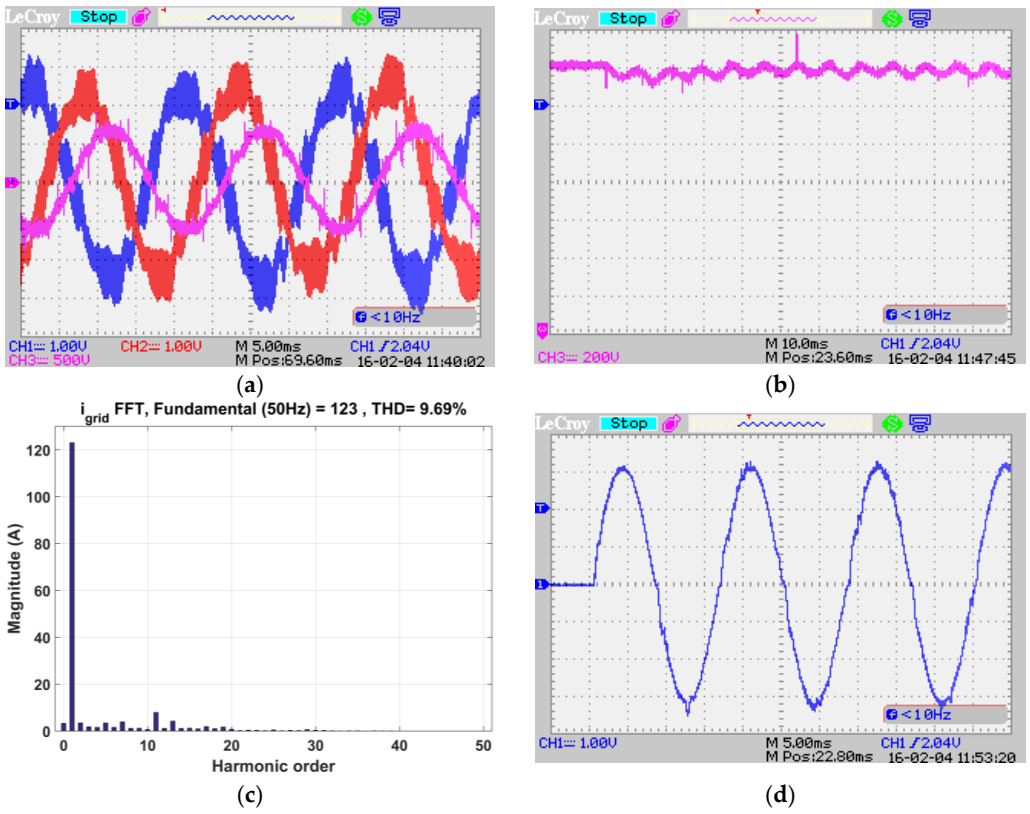


Figure 9. Test results: (**a**) Two phases of grid currents (blue and red), one phase of the grid voltage corresponding to blue current (pink). Vertical sensitivities: CH1 and CH2 = 50 A/div, CH3 = 250 V/div; and (**b**) DC bus voltage. Vertical sensitivity CH3 = 100 V/div; (**c**) Harmonic spectrum of one of the grid current (blue curve of the Figure 9a); and (**d**) the output current at 2.25 kVA. Vertical sensitivity CH1 = 50 A/div.

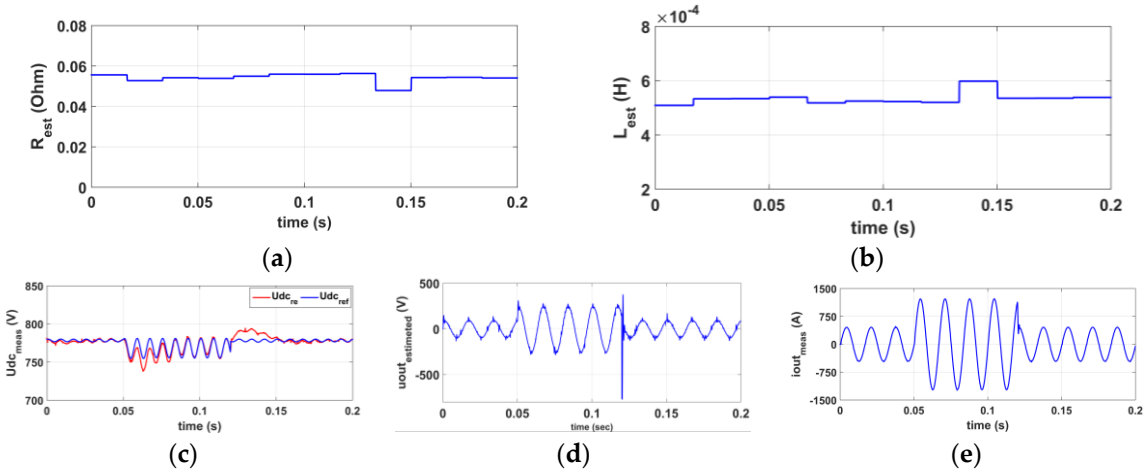


Figure 10. Waveforms on the prototype plotted with samples recorded in the digital signal processor (DSP). (**a**) Estimated resistance over time; (**b**) estimated inductance over time; (**c**) reference of the DC bus voltage (blue), real DC bus voltage (red); (**d**) the fundamental of the output voltage estimated; and (**e**) the output current.

4.2. Welding Test with the Converter

The welding test has been performed on a functional RSEW system where its traditional power converter has been replaced by the prototype presented in Figure 8. The effective value of the output current required to perform a barrel weld was about 500 A. The whole welding system and the barrel welded when using the prototype as the power converter are presented at the Figure 11.

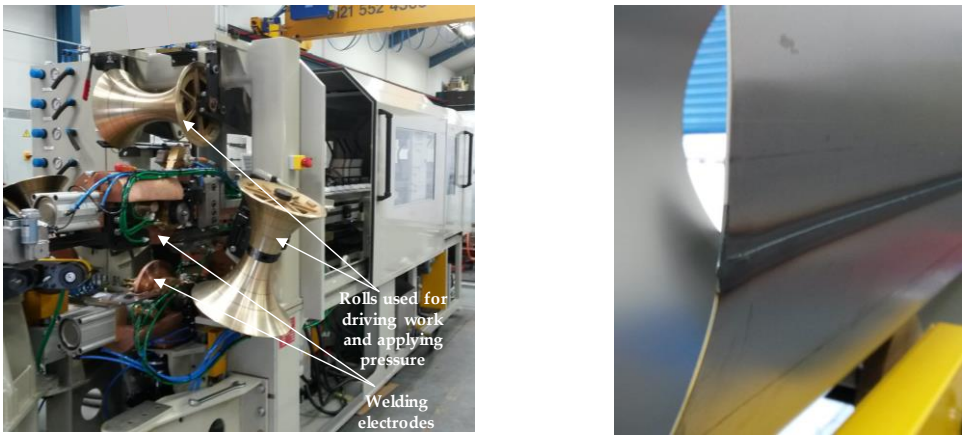


Figure 11. Resistance seam welding system. (**a**) Whole welding system; and (**b**) a barrel welded with the prototype as the power converter.

The whole welding process is carried out in approximately 7 s. Figure 12 presents the estimated parameter's traces during the welding process. Figure 12a presents the fundamental of the output voltage and the output current traces during the welding process used for the output power estimation (a section between t = 1 s and t = 1.5 s). Figure 12b presents the estimated active power at the output of the converter, whereas Figure 12c,d present the estimated load resistance and inductance, respectively. From t = 0 s to t = 0.8 s, the system is in idle state. Output resistance and inductance preset values are about 0.132 Ω and 1.5 mH, respectively. From t = 0.8 s to t = 2.6 s, the converter enters into normal operation. The welding electrodes are joined, but without the barrel to weld. A current is flowing between the electrodes and a power of about 36 kW is delivered at the output of the converter.

At t = 2.6 s, the barrel to weld begins to flow between the welding electrodes. The output power of the converter steps from 36 kW to 46.5 kW (Figure 12b) and, hence, a useful power of about 10 kW for the welding. The output resistance is estimated over time, in steps from 0.13 Ω to 0.18 Ω (Figure 12c) and the estimated output inductance, which was decreasing, steps from 1.58 mH to 1.61 mH (Figure 12d). One can observe that the output parameters vary when the welding starts and during the welding process. This justifies a suitable estimation of those parameters over time and their integration into the control scheme.

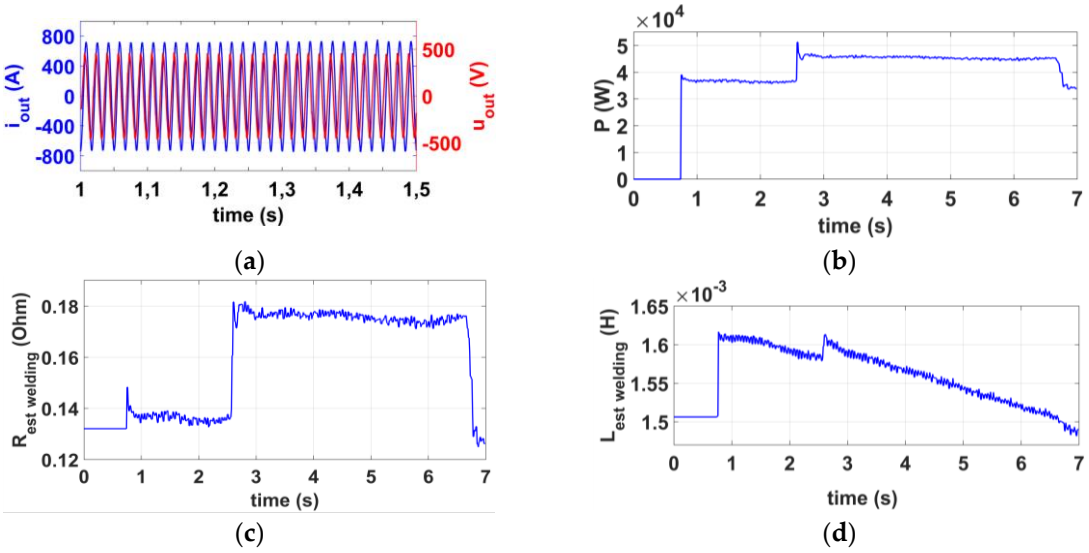


Figure 12. Waveforms of the estimated output parameters during welding process. (**a**) Output current measured (blue trace) and fundamental of the output voltage estimated (red trace); (**b**) output active power; (**c**) estimated output resistance during welding process; and (**d**) estimated output inductance during welding process.

5. Conclusions

This paper explores the control of a three-phase to single-phase back-to-back converter to achieve both a unit power factor and constant power on the utility grid and output regulated parameters for electrical resistance welding applications. The proposed control strategy is to vary the DC link voltage to manage the variations generated by the load, avoiding their propagation on the feeder side. A suitable estimation of the load parameters is also performed to handle the case of load variations. Simulation results proved that by allowing the DC link voltage to vary in a suitable manner, the requirement in terms of power factor can be achieved at the point of common coupling. Moreover, these simulation results have shown that taking into account the load variations in the control scheme can reduce the THD of grid currents by more than 80%. Tests have been carried out on a dummy load and on a real resistance seam welding machine. Both tests have confirmed good functioning of the estimation scheme and, hence, the effectiveness of the proposed control strategy.

Author Contributions: Simon Kissling initiated the study, designed the system and carried out experimental tests. Elie Talon Louokdom, Frédéric Biya-Motto and Bernard Essimbi Zobo performed the mathematical analysis of the converter and developed the simulation model. Elie Talon Louokdom analyzed the simulations and test results data. Mauro Carpita coordinated all the project's activities starting from the design of the system to the experimental tests and the paper writing. All the authors equally contributed to the paper writing.

Conflicts of Interest: The authors declare no conflict of interest.

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