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Editorial

Applications Enabled by FPGA-Based Technology

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Field-programmable gate array (FPGA) technology represents a potential alternative to classical CPUs and GPUs in the post-Moore era from edge computing to data centers. FPGAs offer performance improvements when compared with traditional processing architectures due to their spatial computation capability and energy efficiency. In recent years, FPGA technologies have evolved in different forms of tools, design methodologies, and architectural features. These technologies have enabled or boosted novel application domains. This Special Issue aims to present how advances in FPGA-based technologies have made it possible for multiple application domains.

The following two papers "FPGA-Based High-Throughput Key-Value Store Using Hashing and B-Tree for Securities Trading System" and "Acceleration of Trading System Back End with FPGAs Using High-Level Synthesis Flow" show how FPGA-based technology helps accelerate high-performance trading systems. In first paper, the authors propose a high-throughput key-value store (KVS) for securities trading system applications using an FPGA. The design uses a combination of hashing and B-Tree techniques and supports a large number of keys (40 million), as required by the trading system. The design uses high bandwidth memory (HBM), on-chip memory available in Virtex Ultrascale+ FPGAs, to support a large number of keys. The second paper presents the design of a financial trading system order-processing component using FPGAs, and it was implemented with high-level synthesis (HLS) flow. The order processing component is the major contributor to increased delays and low throughput in the current software implementation of trading systems. The objective of FPGA implementation is to reduce the latency of order processing and increase the throughput of trading systems as compared to software implementation. This paper shows more than double the advantage in order-processing speed and a reduction in latency when using FPGA technology.

FPGA-based applications for machine learning are of a different variety, as shown by "Electromyogram (EMG) Signal Classification Based on Light-Weight Neural Network with FPGAs for Wearable Application", "An Instruction-Driven Batch-Based High-Performance Resource-Efficient LSTM Accelerator on FPGA, and "Improving Seed-Based FPGA Packing with Indirect Connection for Realization of Neural Networks" . In the first paper, to accomplish a lightweight neural network, a maximal overlap discrete wavelet transform (MODWT) and a smoothing technique were used for better feature extractions. Moreover, learning efficiency increased when using an augmentation technique. In designing the neural network, a one-dimensional convolution layer is used to ensure that the neural network is simple and lightweight. Consequently, the lightweight attribute can be achieved, and neural networks can be implemented in edge devices such as the FPGA, yielding low power consumption, high security, fast response times, and high user convenience for wearable applications. The second paper proposes an LSTM accelerator that is driven by a specific instruction set. The accelerator consists of a matrix multiplication unit and a post-processing unit. The matrix multiplication unit uses the staggered timing of read data to reduce register usage. The post-processing unit can complete various calculations with only a small amount of digital signal processing (DSP) slices using resource sharing, and at the same time, the memory footprint is reduced via well-designed data flow

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Citation: Guerrieri, A.; Upegui, A.; Gantel, L. Applications Enabled by FPGA-Based Technology. *Electronics* **2023**, *12*, 3302. https://doi.org/10.3390/electronics12153302

Received: 25 July 2023
Accepted: 27 July 2023
Published: 1 August 2023

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designs. The accelerator is batch-based and capable of computing data from multiple users simultaneously. Since the calculation process of LSTM is divided into a sequence of instructions, it is feasible to execute multi-layer LSTM networks and large-scale LSTM networks. Experimental results show that the accelerator can achieve a performance of 2036 GOPS at 16-bit data precision while having higher hardware utilization compared to previous work. The third paper proposed a quantitative rule for packing the priority of neural network circuits and optimized traditional seed-based packing methods using special primitives. The experimental result indicates that the proposed packing method achieves an average decrease of 8.45% in critical path delay compared to the VTR8.0 on Koios deep learning benchmarks.

Furthermore, FPGA-based technology for accelerating algorithms is shown in the following papers. "A Model of Thermally Activated Molecular Transport: Implementation in a Massive FPGA Cluster" reports a massively parallel implementation of Boltzmann's thermally activated molecular transport model. This model allows considering potential energy barriers in molecular simulations and thus modeling thermally activated diffusion processes in liquids. The model is implemented as an extension to the basic dynamic lattice liquid (DLL) algorithm on ARUZ, a massively parallel FPGA-based simulator located at BioNanoPark Lodz. The advantage of this approach is that it does not use any exponentiation operations, minimizing resource usage and allowing one to perform simulations containing up to 4,608,000 nodes. "FPGA Implementation of Shack–Hartmann Wavefront Sensing Using Stream-Based Center of Gravity Method for Centroid Estimation" presents a quick and reconfigurable architecture for Shack–Hartmann wavefront sensing implemented on FPGA devices using a stream-based center of gravity to measure spot displacements. By calculating the center of gravity around each incoming pixel using optimal window matching with respect to the spot size, the common trade-off between noise and bias errors and dynamic range due to window size existing in conventional center of gravity methods is avoided. In addition, the accuracy of centroid estimation is not compromised when the spot moves to or even crosses the sub-aperture boundary, leading to an increased dynamic range. The calculation of the centroid begins when the pixel values are read from an image sensor, and further computations, such as slope and partial wavefront reconstruction, follow immediately as the sub-aperture centroids are ready. The result is a real-time wavefront sensing system with very low latency and high measurement accuracy that is feasible for targeting low-cost FPGA devices. This architecture provides a promising solution that can cope with multiple target objects and work in moderate scintillation.

"FPGA-Flux Proprietary System for Online Detection of Outer Race Faults in Bearings" introduces an online fault detection mechanism for industrial machinery, such as induction motors or their components (e.g., bearings). Most commercial equipment provides general measurements and not a diagnosis. On the other hand, commonly, research studies that focus on fault detection are tested offline or over processors that do not comply with an online diagnosis. In this sense, the present work proposes a system based on a proprietary FPGA platform with several developed IP cores and tools. The FPGA platform and a stray magnetic flux sensor are used for the online detection of faults in the outer race of bearings in induction motors. The integrated parts comprising the monitoring system are the stray magnetic flux triaxial sensor, several developed IP cores, an embedded processor for data processing, and a user interface where the diagnosis is visualized. The system performs the fault diagnosis via a statistical analysis as follows: First, a triaxial sensor measures the stray magnetic flux in the motor's surroundings (this flux will vary as symptoms of the fault). Second, an embedded processor in an FPGA-based proprietary board drives the developed IP cores in calculating statistical features. Third, a set of ranges is defined for the statistical features' values, and it is used to indicate the condition of the bearing in the motor. The results demonstrate that the values of the root mean square (RMS) and kurtosis, extracted from the stray magnetic field from the motor, provide a reliable diagnostic of the analyzed bearing. The platform is based on FPGA XC6SLX45 Spartan 6 of Xilinx, and the architecture of the modules used is described in HDL.

"Finding the Top-K Heavy Hitters in Data Streams: A Reconfigurable Accelerator Based on an FPGA-Optimized Algorithm": This paper presents a novel approach for accelerating the top-k heavy hitter query in data streams using field programmable gate arrays (FPGAs). Current hardware acceleration approaches rely on the direct and strict mapping of software algorithms into hardware, limiting their performance and practicality due to the lack of hardware optimizations at an algorithmic level. The presented approach optimizes a well-known software algorithm by carefully relaxing some of its requirements to allow for the design of a practical and scalable hardware accelerator that outperforms current state-of-the-art accelerators while maintaining near-perfect accuracy. This paper details the design and implementation of an optimized FPGA accelerator that is specifically tailored for computing the top-k heavy hitter query in data streams. The presented accelerator is entirely specified at the C language level and is easily reproducible with high-level synthesis (HLS) tools. Implementation on Intel Arria 10 and Stratix 10 FPGAs using the Intel HLS compiler showed promising results—outperforming prior state-of-the-art accelerators in terms of throughput and features.

Finally, the last two papers presented FPGA-based technology applied to real-time and embedded systems. The first paper, "A New FPGA-Based Task Scheduler for Real-Time Systems" demonstrates a novel design of an FPGA-implemented task scheduler for real-time systems that supports both aperiodic and periodic tasks. The periodic tasks are automatically restarted once their period has expired without any need for software intervention. The proposed scheduler utilizes the earliest deadline first (EDF) algorithm and is optimized for multi-core CPUs that are capable of executing up to four threads simultaneously. The scheduler also provides support for task suspension, resumption, and enabling inter-task synchronization. The design is based on priority queues, which play a crucial role in decision making and time management. Thanks to the hardware acceleration of the scheduler and the hardware implementation of priority queues, it operates in only two clock cycles regardless of the number of tasks in the system. The results of the FPGA synthesis, performed on an Intel FPGA device (Cyclone V family), are presented in the paper. The second paper is "Accurate Multi-Channel QCM Sensor Measurement Enabled by FPGA-Based Embedded System Using GPS" : This paper presents a design and implementation proposal for a real-time frequency measurement system for high-precision, multi-channel quartz crystal microbalance (QCM) sensors using a field programmable gate array (FPGA). The key contribution of this study lies in the integration of a frequency measurement and mass resolution computation based on global positioning system (GPS) signals within a single FPGA chip, utilizing I/O blocks to incorporate logical QCM oscillator circuits. The FPGA design enables parallel processing, ensuring accurate measurements, faster calculations, and reduced hardware complexity by minimizing the need for external components. As a result, a cost-effective and accurate multi-channel sensor system is developed, serving as a reconfigurable standalone measurement platform with communication capabilities. The system is implemented and tested using the FPGA Xilinx Virtex-6, along with multiple QCM sensors. The implementation on a Xilinx XC6VLX240T FPGA achieved a maximum frequency of 324 MHz and consumed a dynamic power of 120 mW. The proposed system meets the precision measurement requirements for QCM sensor applications, exhibiting low measurement errors when monitoring QCM frequencies that range from 1 to 50 MHz with an accuracy of 0.2 ppm and less than 0.1 Hz.

These papers demonstrate the diverse range of applications enabled by FPGA-based technology. As the application requiring high performance and flexibility continues to evolve, we can expect to see even more and more applications in the future.

List of Contributions:

1. Puranik, S.; Barve, M.; Rodi, S.; Patrikar, R. FPGA-Based High-Throughput Key-Value Store Using Hashing and B-Tree for Securities Trading System.
2. Puranik, S.; Barve, M.; Rodi, S.; Patrikar, R. Acceleration of Trading System Back End with FPGAs Using High-Level Synthesis Flow.

3. Jabłoński, G.; Amrozik, P.; Hałagan, K. A Model of Thermally Activated Molecular Transport: Implementation in a Massive FPGA Cluster.
4. Choi, H. Electromyogram (EMG) Signal Classification Based on Light-Weight Neural Network with FPGAs for Wearable Application.
5. Kong, F.; Cegarra Polo, M.; Lambert, A. FPGA Implementation of Shack–Hartmann Wavefront Sensing Using Stream-Based Center of Gravity Method for Centroid Estimation.
6. Mao, N.; Yang, H.; Huang, Z. An Instruction-Driven Batch-Based High-Performance Resource-Efficient LSTM Accelerator on FPGA.
7. Kohútka, L.; Mach, J. A New FPGA-Based Task Scheduler for Real-Time Systems.
8. Cureño-Osornio, J.; Zamudio-Ramirez, I.; Morales-Velazquez, L.; Jaen-Cuellar, A.; Osornio-Rios, R.; Antonino-Daviu, J. FPGA-Flux Proprietary System for Online Detection of Outer Race Faults in Bearings.
9. Ebrahim, A. Finding the Top-K Heavy Hitters in Data Streams: A Reconfigurable Accelerator Based on an FPGA-Optimized Algorithm.
10. Bourennane, A.; Tanougast, C.; Diou, C.; Gorse, J. Accurate Multi-Channel QCM Sensor Measurement Enabled by FPGA-Based Embedded System Using GPS.
11. Yu, L.; Guo, B.; Zhi, T.; Bai, L. Improving Seed-Based FPGA Packing with Indirect Connection for Realization of Neural Networks.

Conflicts of Interest: The authors declare no conflict of interest.

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