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On the Cosmic Ray Influence on the Electronics Design of a High Altitude Electric Aircraft

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Keywords

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Abstract

Space in Earth's orbit is growing more and more scares. High altitude solar electric drones, known as High Altitude Pseudo-Satellites (HAPS), are becoming a viable solution to replace satellite functions. One of the issues that must be faced in their design are cosmic rays (CR). CR can cause failures in power electronics and their flux is significantly higher with altitude. Additionally, with lower pressures, arcing and thermal management become issues as well. This study aims to determine the effects of cosmic radiation at stratospheric altitudes and fix guidelines to be able to answer how to design a high-altitude electric aircraft power plant.

Introduction

Space junk is becoming a risk issue for the satellite services, on which our modern society depends on and having an alternative is critical. One solution that is being investigated is in the form of high-altitude pseudo-satellite (HAPS) stratospheric drones. Currently, the stratosphere is a flight domain which is not or only very little exploited. The airspace is controlled up to FL660 (20.1km), which is just above the Armstrong limit, altitude at which a short decompression event would be lethal for a human being. However, most of the traffic is below FL400 (12.2 km). In fact, commercial airliners are designed to fly close to the tropopause to avoid weather as well as for speed. The technology readiness for perpetual electric flight has been demonstrated with the Solar Impulse project [1] which was concluded in 2016. Private endeavors such as Airbus's Zephyr [2] are now exploring the field. The targeted altitudes require special attention due to the harsh stratospheric conditions, such as cosmic ray radiation levels that are two to three orders of magnitude higher than at sea level, as well as the issues liked to the low-pressure environment. The goal here is to provide design guidelines to solve or mitigate the issues caused by the CR, to be able to design a reliable high-altitude electric power plant. Part of the work presented here is supported by the Swiss Federal Office of Energy in a demonstration project where the strategies and components for the future electrification of aeronautical power and propulsion systems is investigated [3]. The paper begins by presenting the structure of the power plant under investigation and then by explaining the methodology to be applied. Then, the preliminary results are presented, and design recommendations are discussed.

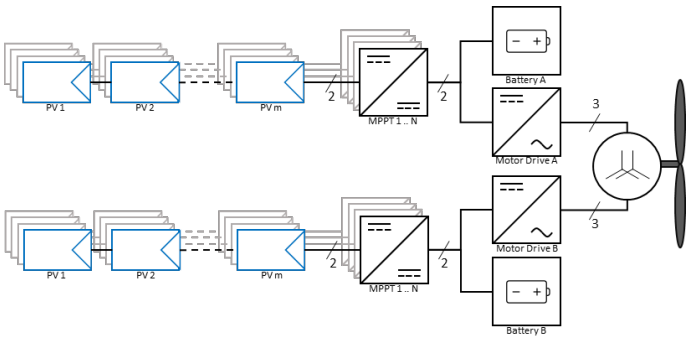

Fig. 1: Block diagram of the proposed power plant. Two independent power systems drive one motor with electrically insulated double windings.

General structure of the power plant

The general structure of the proposed power plant is illustrated in Fig. 1. A design composed of two fully independent power drive systems in parallel which drive one motor with electrically insulated double windings has been chosen. Each system has its own photovoltaic (PV) energy supply chain and battery pack. In case of one side failing, the other can still provide half the power, allowing for safer return. The chosen system voltage is based on a battery composed of 96 lithium-ion cells in series. This choice is motivated by geometric flexibility of the battery pack, since 96 is a multiple of ten different integers. Furthermore, the resulting voltage level (290-400V) is a good compromise in terms of efficiency. Is high enough to improve efficiency, yet low enough for component technology and availability to enable implementation. It must be remarked that this also corresponds to the battery configuration of the Pipistrel VELIS Electro, the first and currently only type-certified electric aircraft in the world [4]. In this paper, examples we will be specially concentrated around the design of the motor drive. However, the same principles apply to the DC/DC MPPT converters.

Methodology

The effects of CR on electronics have been studied since they were suspected and confirmed in the 1980s [5]. In the beginning of the 1990s, experiments at the surface and in a salt mine 140m below showed that the failure in time (FIT) of power devices such as GTO's and IGBT's was exponentially dependent on the applied voltage and could be attributed to CR [6]. Observation of MOSFET failures due to high energy neutrons soon followed [7]. CR are known to cause single event effects (SEE) [8]–[12] that, depending on the device can cause soft errors, such as bit-flips, or hard errors, such as single event burnouts (SEB). Neutrons, protons and pions are known to be the main source of SEEs at ground level [13], however at higher altitudes, heavy ions can also participate in the disturbance. Because of the high energy levels of CR, as well as the weight constraint on aircrafts, possible shielding has limited effect. CR must be delt with rather than attenuated. To be able to determine the effects of CR on the electronic devices at high altitudes, it is imperative to know the nature of the radiation. The EXPACS [14] tool, cited as a reference source by IEC 62396-1:2016 [13], allows to simulate the differential particle flux (Fig. 2) for different particles at different altitudes and different geomagnetic cutoff rigidities [15].

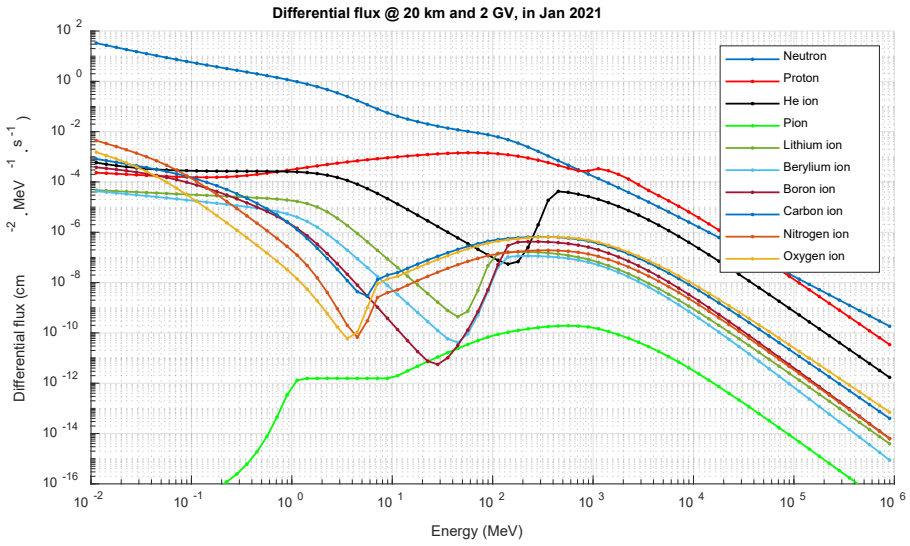

Fig. 2: Differential particle flux at an altitude of 20 km and a cutoff rigidity of 2 GV in January 2021

Since the goal here is to design a power plant allowing perpetual electric flight, the latitude north and south of the equator is limited to a certain range because of the apparent height of the Sun. The study being CR, this limit can be described as a minimum vertical geomagnetic cutoff rigidity (as the vertical cutoff rigidity is maximum close to the equator and reduces to almost zero at the poles). In the present study, this minimum was chosen to be 2 GV.

Hereafter, there are three category issues that need to be addressed: i) Single Event Effects (SEE) on the information level (signal or memory) where errors can be addressed through redundancy and error detection, ii) Single Event Burnouts (SEB) and Single Event Gate Rupture (SEGR), which are hard errors that can have catastrophic consequences and need to be avoided through adequate sizing and derating, and iii) Total Ionizing Dose (TID) and displacement damage, which are the result of long term radiation exposure and determine a maximum lifespan base on experimental observations.

Single Event Effects

The effects of CR are different depending on the size and type of electronic component. Two energy thresholds are defined as significant in [13] depending on component feature size. For devices with feature sizes smaller than 150 nm, the threshold is set to 1 MeV, above it is set to 10 MeV. The particle fluxes with energies higher than the threshold is obtained by integrating the differential flux above the preset energy threshold. Data was extracted from EXPACS ranging from sea level up to an altitude of 50 km. The same was done over a whole time period ranging from 1950 to 2021 to observe the effect of the solar cycles. At solar minimum (low Sunspot count), the particle flux is at its highest, and vice versa. Fig. 3 shows the calculated fluxes with the two predefined thresholds, in January 2021, during a solar minimum. At solar maximum, depending on the intensity, the flux can be attenuated by 50%.

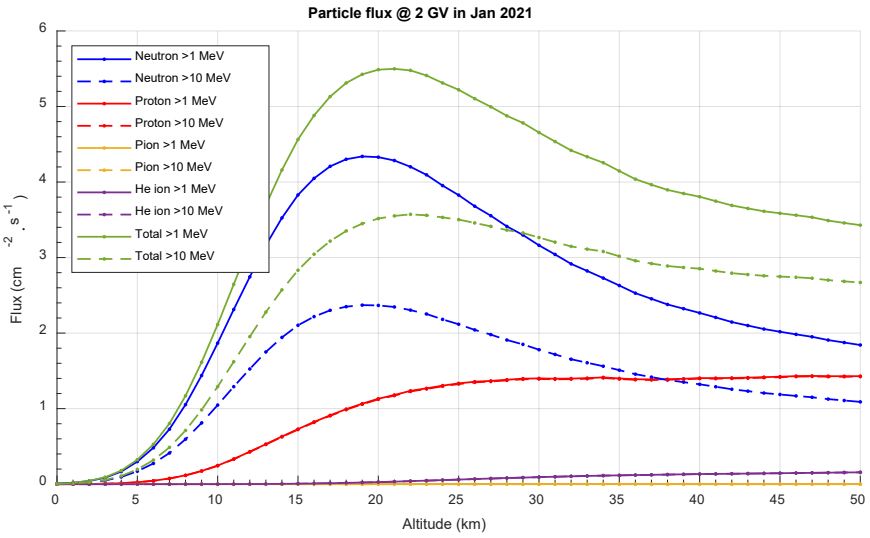

Fig. 3: Particle flux as a function of altitude, with energies greater than 1 MeV and 10 MeV for a cutoff rigidity of 2 GV in January 2021.

The abundance of particles with energies higher than 1 MeV is significantly greater than the particles with energies greater than 10 MeV. However, as shown in Fig. 3, the difference is entirely in the abundance of neutrons. The total flux at the peak is 700 to 800 times greater than at sea level. To calculate the upset rate (1), the cross section of the a given device must be known. This is determined experimentally for each component in a particle accelerator.

$$\text{Upset rate } [\text{s}^{-1}] = \text{Flux } [\text{cm}^{-2} \cdot \text{s}^{-1}] \cdot \text{Bit X-section } [\text{cm}] \quad (1)$$

In [16], cross sections for different memory chips where measured as a function of proton energy as well as linear energy transfer (LET) for different heavy ions. What comes out is that cross section is strongly dependent on LET. What also appears, is that the cross sections for protons peaks at approximately the physical cross section of the memory bits and is otherwise three to four orders of magnitude lower. The cross section for heavy ions can be a thousand times more than the physical cross section, however they are also much less abundant.

In their experiments, the cross section for protons peaks around 1 MeV, which certainly corresponds to the specific energy for the proton's Bragg peak to occur in the sensitive area of the tested memory chips. Neutrons do not ionize directly since they do not experience the electronic stopping power (responsible for the Bragg peak). However, they produce secondary protons though nuclear collisions, which do. Simulations performed with SPENVIS [17] show that the interactions between neutrons and matter produce secondary protons are between two to four orders of magnitude less abundant than the neutrons. In any case, when using off the shelf components, few will have been tested to determine their cross sections and the information is usually not readily available. However, a worst-case scenario can be done by considering the total flux with energies above 1 MeV and the physical cross section. For example, considering a 50 KB RAM memory on a microcontroller and a 100 nm^2 cross section per bit, the total cross section is $4 \cdot 10^{-7}$ cm^2. With 5.5 particles cm^2/s, there would be an average of 69 upsets per year. This shows that even with a conservative approach, the upset rate is extremely low in regard of the microcontroller's clock frequency, however measures must be taken to make the system as robust and error proof as possible.

Single event burnout and single event gate rupture

SEEs, as presented above, are at a signal or information (memory) level and are in a low voltage environment. A SEB concerns power semiconductors which withstand large voltages and where the active part is subject to high electric fields. SEB occurs when a power semiconductor such as an IGBT or a MOSFET is off (blocking) and suffers catastrophic failure due to an ionizing particle (usually a heavy ion) causing it to switch on at an undesired moment. Concretely, the deposition of charge caused by the particle penetrating the drain-body-source region causes a partial forward bias in the junction. If the drain-source voltage (V_{DS}) is high enough, the remaining blocking part of the junction breaks down and current rushes through, leading to burnout. SEB occurs at drain-source voltages lower than the rated voltages of commercial components. The probability of destruction by cosmic radiation is reduced by manufacturers of power semiconductors thanks to the dimensioning rules for the thickness and the distribution of the electric field in the components. On the ground, these rules specify a random failure rate of approximately 1–3 FIT per cm^2 of component surface, or 1 to 3 failures per billion hours of operation and cm^2 [18]. Protons and neutrons have also been shown to cause SEB and extensive research has been done to determine the safe derating levels at which no SEB has been observed [19]–[25]. These studies show that a derating from 80% to 50% reduces FIT by a factor 1000x [20]. Since at stratospheric altitudes the particle flux is 700 to 800 times higher than on the ground, derating should be further down at 33%. Furthermore, in support of this recommendation, it has been shown that SEB does not occur below 400V with 1200V SiC MOSFETs [24]. P-channel MOSFETS are almost immune to SEB [26], however their downside is that their internal resistance is approximately three times higher due to the difference in carrier mobility.

SEGR affects as much N-channel than P-channel power semiconductors. It occurs when a heavy ion strikes a MOSFET through the gate oxide region [27]. The ionized track leads to a localized increase in the oxide field which causes it to breakdown. Leakage starts to occur until rupture of the gate. Some events that appear to be SEB are actually caused by SEGR [28]. SEGR had been thought to be caused only by heavy ions, however it has be shown that high energy protons [29] as well as neutrons can also be the cause [30]. The only way to reduce the risk of SEGR is through derating [31].

Total Ionizing Dose

Total ionizing dose is the cumulative effect due to exposition to ionizing radiation. All particles participate in the total ionizing dose. The observable effect is a gradual degradation of the electrical properties of an electronic device. TID affects as much metal oxide semiconductors (MOS) as bipolar devices. The main effects are increased leakage currents, change of threshold voltages and degraded timing [32]. Based on more than two decades of experimental results, the lower boundary at which devices still perform within specifications has been found to be 10 Gy (J/kg) [13]. However, most components can withstand much more. IEC 62396-1:2016 [13] recommends setting the TID threshold for avionics at 5 Gy.

To calculate TID, a tool such as SPENVIS can be used, however the environment and the geometry around each component must be known. Since this is not feasible here, a specific case is studied to see what the TID levels are. Simulations were done considering a 2 mm thick aluminum sheet (airframe, and electronics casing) and a 0.2 mm thick silicon wafer. The differential flux shown in Fig. 2 was used as input data and setup omnidirectionally. Table 1 summarizes the results.

Protons	2.176 µGy/h	Helium ions	0.356 µGy/h	Nitrogen ions	0.038 µGy/h
Neutrons	0.252 µGy/h	Lithium ions	0.005 µGy/h	Oxygen ions	0.179 µGy/h
Electrons	0.901 µGy/h	Beryllium ions	0.006 µGy/h	Fluorine ions	0.006 µGy/h
Positrons	0.734 µGy/h	Boron ions	0.033 µGy/h	Neon ions	0.026 µGy/h
Gamma rays	0.476 µGy/h	Carbon ions	0.096 µGy/h	Sodium ions	0.007 µGy/h

Table 1: Ionizing dose, by particle, absorbed by the 0.2 mm silicon wafer, calculated using SPENVIS, with the cosmic ray data extracted from EXPACS, at an altitude of 20 km and a vertical cutoff rigidity of 2 GV, in January 2021.

The contributions of the heavy ions were calculated up to aluminum. The total ionizing dose calculated for all the particles in Table 1 sums up to 5.35 µGy/h. Rounding up to 6 µGy/h, it would take 95 years to reach the 5 Gy threshold. Changing the thickness of the silicon or the shielding changes only a little the TID. E.g., exposing directly a 1 mm thick silicon wafer without shielding results in a TID of 5.72 µGy/h. It is safe to say that TID is not an issue in the present study in normal operating conditions.

Displacement damage

Displacement damage refers to atoms being knocked out of their lattice by an energetic particle. It is a cumulative effect, as TID, however it is mainly due to heavy ions, protons and neutrons. Past a certain threshold, displacement damage causes electronic devices to no longer function normally. The threshold was defined experimentally on sensitive optocouplers with a 1 MeV equivalent neutron fluence at 10^{10} neutron/cm^2 [13]. MOS devices have a much higher threshold of 10^{15} neutron/cm^2 [26]. Two methods are used to calculate displacement damage.

The first method uses the non-ionizing energy loss (NIEL) function [33], [34], which is accepted as the best estimate of the potential displacement damage. NEIL, or D, is dependent on the nature of the incoming particle and its energy. According to ASTM E722-19 [35], the displacement damage cross section for a 1 MeV neutron, noted $D_n(1\ MeV)$, is 95 MeVmb. This value is defined as the normalizing value. NEIL scaling of any particle, with any energy, is then expressed in terms of hardness factor k, where:

$$k_{particle} = \frac{D_{particle}}{D_n(1\ MeV)} \tag{2}$$

Therefore, the hardness factor $k_{particle}$ is the displacement damage relative to a 1 MeV neutron. Using hardness data of neutrons and protons from [36] and applying it to their respective differential fluxes at 21 km, we obtain the $D_n(1\ MeV)$ equivalent differential flux (Fig. 4). These are then integrated over the full available energy spectrum to obtain the $D_n(1\ MeV)$ equivalent flux (Fig. 5).

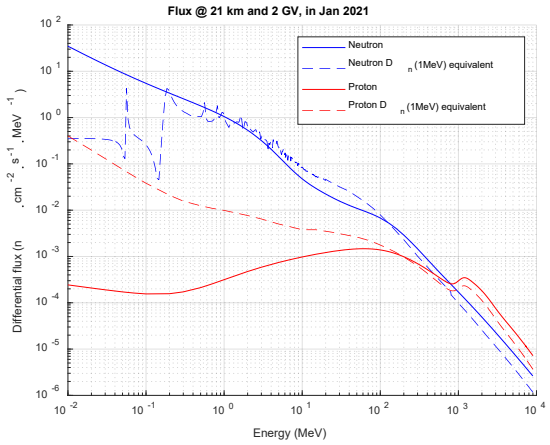

Fig. 4 : Neutron and proton differential fluxes and their respective resulting differential displacement damage fluxes.

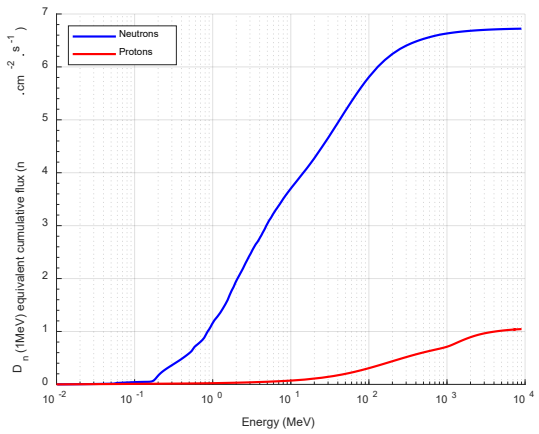

Fig. 5: $D_n(1\ MeV)$ equivalent cumulative flux for neutrons and protons.

The total $D_n(1\ MeV)$ equivalent cumulative flux adds up to 7.75 $[n \cdot cm^{-2} \cdot s^{-1}]$. Rounding up to 10, to take into account heavy ions, results in a lifespan of over 277'000 hours (31 years).

The second method is a much simpler one and is the one proposed in IEC 62396-1:2016. This method only considers the neutron flux between 1 MeV and 1 GeV and applies a factor of three as a conservative measure. At an altitude of 21 km the neutron flux with energies between 1 MeV and 1 GeV is 4.3 neutron $\cdot$ cm^{-2} $\cdot$ s^{-1}. With the factor three, it takes more than 215'000 hours of flight at 21 km to reach the fluence threshold. This second method is indeed more conservative then the first. Nevertheless, even with the conservative method, displacement damage is yet not an issue before more than 24 years.

Summary and design recommendations

As shown, SEEs are present, but not at a high frequency. SEEs group several different effects. Among these are single event upsets (SEU), multiple bit upsets (MBU), multiple cell upsets (MCU), single event transients (SET), single event functional interrupt (SEFI) and single event latch up (SEL). These are all non-destructive and are reversible. Single event burnout (SEB), single event gate rupture (SEGR) and single event induced hard error (SHE) are all permanent damage.

SEU refers to a single bit being flipped in a memory, where the effect is reversible by rewriting the bit. This can be solved though simple error detection and correction algorithms. However, it will be shown further that more advanced error correction algorithms are necessary.

MBU and MCU are caused by a shower of secondary particles, originating from the same primary particle, which generate multiple simultaneous upsets. MBUs are when multiple bits in a same word are flipped, whereas MCU is when bits in different words are flipped during the same event. For critical functions, static RAM (SRAM) is preferable to dynamic RAM (DRAM) [13]. Because DRAM has space optimization logic, an upset in this logic can cause thousands of bits to be in error because of one event. To minimize the risk of MBU and MCU being an issue, more advanced error detection and correction algorithms, such as Reed-Solomon, are necessary. Furthermore, the memory should be physically distributed in different locations.

CR can also create transient disturbances at the signal level (in operational amplifiers, ADCs, etc.) in which case it is referred to as a SET. These can occur on analog or digital signals and lead to false readings or false commands. When data is being read or processed, repeating operations allows to detect SETs and eliminate them. Furthermore, more robust hardware can be used. To give an example, in the present case, the position sensing of the propeller shaft that is fed to the motor drives is done using a resolver rather than an encoder. Resolvers, though less accurate, are much more robust than encoders.

When sending a command, e.g., to a power device's gate driver, an untimely turn on can have catastrophic consequences. To reduce this risk, gate drivers with both high side and low side signal inputs that reject the command if both signals are high can be used. Furthermore, a hardware short-circuit protection which pulls down the driver command signals can be implemented to further reduce the risk. Additionally, placing a pull-down resistor between the gate and source is always recommendable because it reduces the risk of an EM transient as well as charge deposition from CR to cause MOSFETs to auto-turn on during the high Z state of gate drivers when switching or powered down.
An SEU in the wrong place can cause a complex system such as a microprocessor to misfunction and is qualified as a SEFI. For example, a bit flip in a critical register or a program counter could cause the system to freeze. In some devices such as DRAMs and FPGAs, a SEFI can cause an increase in supply current [13]. A reset or a power cycle may need to be applied to resolve it. Detection and resolving of SEFI is done, depending on how critical the system is, though double or triple modular redundancy. In the current project, the chosen microcontroller is part of the Hercules family by Texas Instruments. This microcontroller has double modular redundancy built in. It is equipped with dual cores that execute the same instructions in parallel. A check is done to control that both results are coherent. Additionally, the two cores are not physically in the same location and are oriented differently to reduce the chances of the same bits being flipped simultaneously.

A SEL is a short circuit that can occur in an integrated circuit (IC). It is caused by the triggering of a parasitic structure that creates a low impedance path short circuiting the power supply. It can rapidly lead to the destruction of the IC. A power cycle is required to resolve the latch-up. A power supply monitoring system with an auto-power cycle must be implemented.

SEB and SEGR only occur on power devices in the off state with a high voltage present between drain and source. Both phenomena are due to a charge deposit that consequently overwhelms the dielectric strength of the device. As shown above, protection against SEB and SEGR can only be done thought appropriate derating. A derating of 33%, corresponding to a usage at 1/3 of the nominal voltage is recommended at stratospheric altitudes.

SHE is when a particle causes a memory bit to be permanently stuck. This significant because it cancels simple error correction codes such as single error correct, double error detect (SECDED). If any other error occurs, it will not be corrected. For this reason, advanced error detection and correction algorithms are again necessary.

Total ionizing dose as well as displacement damage were shown not to be of concern, because even with a conservative calculation, the lifespan is expected to be more than 24 years. However, one of the effects of radiation on power devices is slow but progressive increase in leakage across insulating boundaries. The leakage between drain and gate can cause the gate to charge itself and the device to auto-turn on. To compensate for this leakage, in addition to the pull-down resistor between gate and source, a negative bias voltage should be applied as well.

Conclusion

CR can cause errors, disfunctions of complex electronic systems and can even lead to catastrophic failure of power devices. In order to quantify the risk posed by CR on avionics and power drives functioning at stratospheric altitudes, as well as to minimize it and compensate for the effects, the intensity of the CR was defined as well as their effects on electronic devices. Because of the high energies in play, the effectiveness of shielding to attenuate CR is limited. However, the effects are manageable and solutions exist to correct induced errors and minimize the risk of catastrophic failure. Single event effects are the main issue, whereas long term exposure is less. For each type of effect concrete recommendations were given allowing to define the design guidelines for a high-altitude power electronic system regarding cosmic rays.

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